2822
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PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	

Application Number	08/691,434
Filing Date	August 2, 1996
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2822
Examiner Name	M. Wilczewski
Attorney Docket Number	0756-1551

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition to Withdraw From Issue
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosures
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Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, VA 20165
Signature	*Eric J. Robinson*
Date	10-21-04

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Docket No. 0756-1551

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Shunpei YAMAZAKI et al.)
Serial No. 08/691,434)
Filed: August 2, 1996)
For: METHOD OF FABRICATING)
SEMICONDUCTOR DEVICES AND)
APPARATUS FOR PROCESSING A)
SEMICONDUCTOR)

Art Unit: 2822
Examiner: M. Wilczewski

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The enclosed references were recently cited in a rejection by the Japanese Patent Office in a counterpart Japanese application. The rejection includes the following comments:

With respect to claims 1-5. When comparing an invention claimed in claim 1 of the present application with Japanese Patent Laid-Open No. 63-318125 (This is referred to as cited document 1 hereinafter. Particularly see from page 3, upper left column, line 4 to page 4, upper right column, line 13.), they are different in five points as follows.

(A) In the invention claimed in claim 1 in the present application, a semiconductor film formed on a glass substrate is used for a

channel region of a transistor. On the contrary, in an invention described in the cited document 1, a semiconductor substrate itself is used for a channel region of a transistor.

(B) In the invention claimed in claim 1 in the present application, an N-type impurity is doped. On the contrary, in the invention described in the cited document 1, a P-type impurity is doped.

(C) In the invention claimed in claim 1 in the present application, a gate insulating film in an ion implantation area is removed by dry etching. On the contrary, in the invention described in the cited document 1, a gate insulating film in an ion implantation area is removed by wet etching.

(D) In the invention claimed in claim 1 in the present application, a semiconductor treatment apparatus used in the invention has a first chamber for doping and a second chamber for etching and a third chamber for a laser light irradiation. Further, in the invention claimed in claim 1 in the present application, a treatment substrate is transferred among these chambers without exposing the treatment substrate to an outside air. On the contrary, in the invention described in the cited document 1, it is not expressly described that a treatment substrate is transferred among chambers without exposing the treatment substrate to an outside air.

(E) In the invention claimed in claim 1 in the present application, a laser light is irradiated after etching an insulating film. On the contrary, in an invention described in the cited document 1, a lamp annealing is conducted after etching an insulating film.

The above different points are considered as follows.

With respect to the different points (A) to (C). It is a known technology before filing the present application to use a semiconductor layer formed on a glass substrate for MOS transistor, and to use a dry etching method causing a discharge for an etching method of an insulating film, and to form an N-type transistor doped with an N-type impurity.

With respect to the different point (D). It is a known technology before filing the present application to form a semiconductor device by using a multi-chamber for conducting a successive process without exposing to an outside air to conduct a heat treatment process such as film formation, crystallization or an impurity activation and to conduct an etching, in order to prevent a treatment substrate from being polluted, as described in "NIKKEI MAICRO DEVICE, October, 1989" (This is referred to as cited document 2 hereinafter. Particularly see from page 34 to page 39) cited in the prior rejection and in Japanese Patent Laid-Open No.4-251921 (This is referred to as cited reference 3 hereinafter. Particularly see from the first paragraph to the 41st paragraph) cited in the prior rejection. It is an implementable matter by ordinary skill in the art as occasion demands to conduct steps such as an impurity doping and an insulating film etching and an impurity activation described in the cited document 1 by using a multi-chamber.

With respect to the different point (E). It is merely a known technology before filing the present application to conduct an impurity activation by a laser light, as described for example in Japanese Patent Laid-Open No. 4-221854 (This is referred to as cited document 4 hereinafter. Particularly see the 38th paragraph.) cited in the prior rejection and in Japanese Patent Laid-Open No. 3-201528 (This is referred to as cited document 5 hereinafter. Particularly see from page 3, lower left column, line 4 to page 3, lower left column, line 16) cited in the prior rejection.

The same is applied to claims 2-5.

In this way, the invention claimed in claims 1-5 of the present application involves a matter easily made by one of ordinary skill in the art from the cited document 1 and the above know technologies.

With respect to claim 6. It is merely a known technology before filing the present application to form a mask comprising a resist mask over a first gate electrode so as to cover a first active layer, to conduct a first ion implantation using a second gate electrode provided over a second active layer as a mask, and to conduct a second ion implantation using the first gate electrode over the first active layer and the second gate electrode over the second active layer as masks after removing the resist film over the first gate electrode, as described for example in Japanese Patent Laid-Open No. 3-42868 (This is referred to as cited document 6 hereinafter. Particularly see from page 3, lower left column, line 3 to page 4, upper right column, line 12.) and in Japanese Patent Laid-Open No. 3-95965 (This is referred to as cited document 7 hereinafter. Particularly see from page 2, upper left column, line 15 to page 2, lower left column, line 15).

In addition, it is a known technology before filing the present application to conduct a resist removal by a chamber.

With respect to claim 7, it is described in the cited document 5 to conduct an impurity activation by an excimer laser.

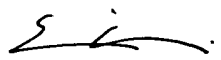
With respect to claim 8, it is merely a known technology before filing the present application to use a liner laser light for a shape of a laser light and to irradiate with a substrate scanned.

In this way, the invention as claimed in claims 1-8 of the present application can be easily invented by one of skill in the art, based on the cited references 1-7.

U.S. Patent No. 5,316,960 is in the family of JP 03-042868. This U.S. Patent was not directly cited by the Japanese Patent Office, but is submitted herewith for consideration by the Examiner.

An RCE was filed in this application on June 9, 2004, and no further Office Action has been received. Therefore no fee is required.

Respectfully submitted,



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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	08/691,434
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Attorney Docket Number	0756-1551

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,316,960		Watanabe et al.	05/31/1994	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	03-042868			02/25/1991		Abst.
		JP	03-095965			04/22/1991		Abst.

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.